Figure 1: prior art VHDL listing

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;                                   100
USE ieee.std_logic_arith.ALL;                                   ↙

ENTITY test IS
        PORT(
                clk : IN std_logic;
                rst : IN std_logic;
                in1 : IN unsigned(7 downto 0);
                in2 : IN unsigned(7 downto 0);
                out1 : OUT unsigned(7 downto 0)
        );
END;

ARCHITECTURE behavioral OF test IS
BEGIN
        main : PROCESS
                VARIABLE min1 : unsigned(7 downto 0);
                VARIABLE min2 : unsigned(7 downto 0);
        BEGIN
                WAIT UNTIL (clk'EVENT and clk = '1');
                min1 := in1;
                min2 := in2;
                loop1 : WHILE ( min1 < min2 ) LOOP
                        IF (min2 > 0) THEN
                        130
                                FOR x IN 0 TO 7 LOOP
                                        min1 := min1 + min2;
                                        min2 := min2 -1;
                                END LOOP;
                        ELSE
                        140
                                FOR x IN 10 DOWNTO 5 LOOP
                                        min1 := min1 - x;
                                END LOOP;
                        END IF;
                END LOOP;
                out1 <= min1 * min2;
        END PROCESS;
END;
```

110 ↙ 120 ↙

Figure 2a: prior art Gantt chart

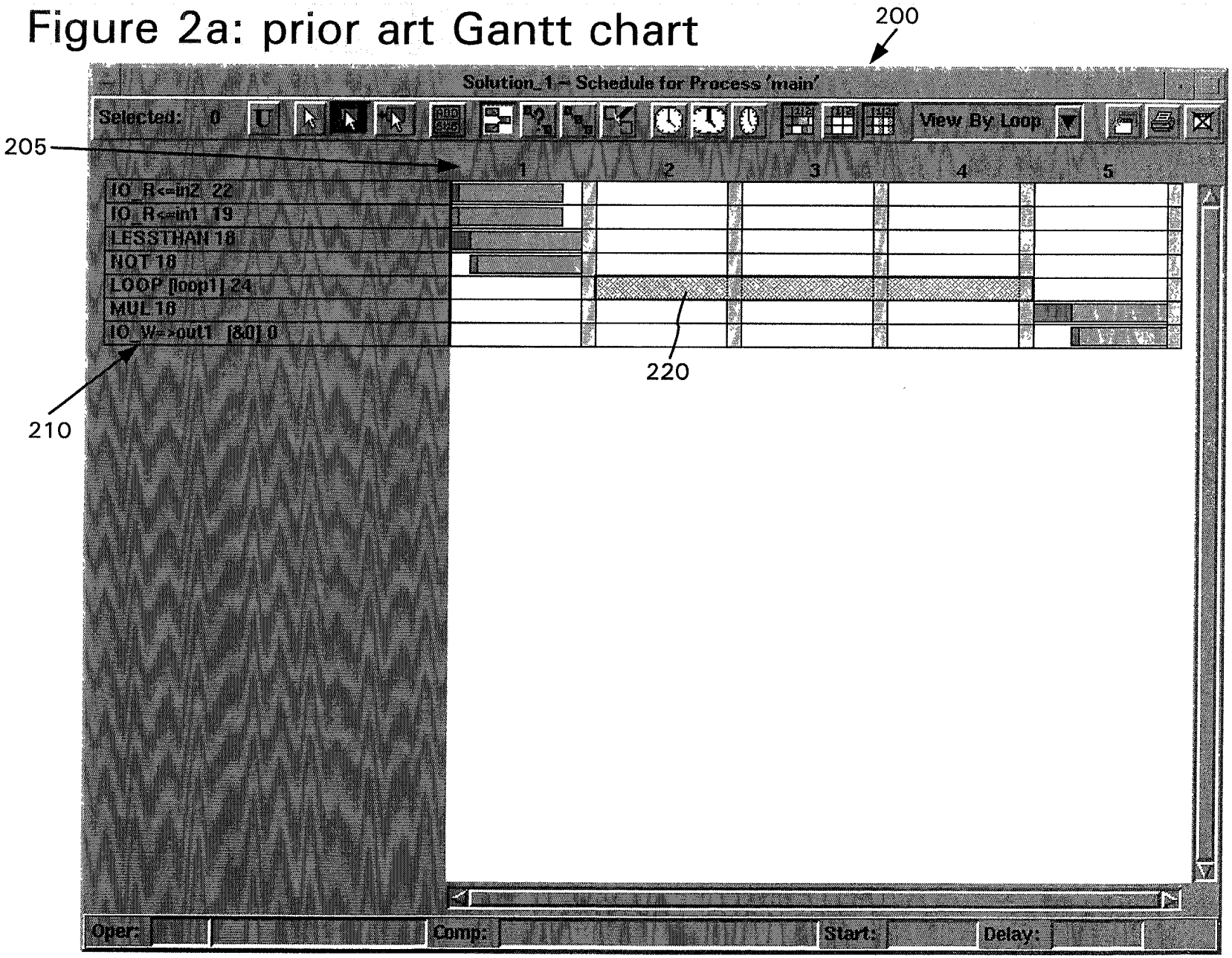


Figure 2b: prior art Gantt chart

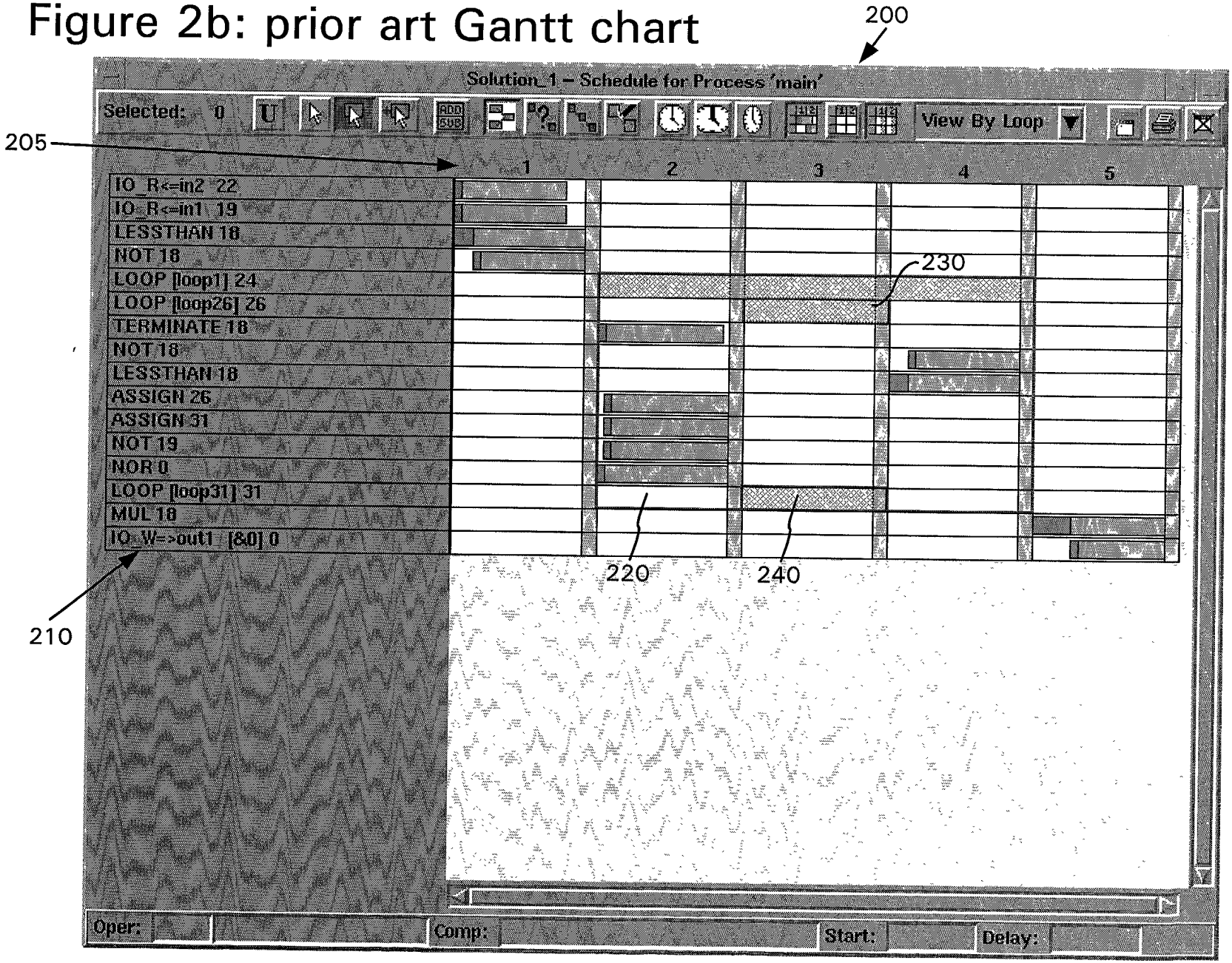


Figure 2c: prior art Gantt chart

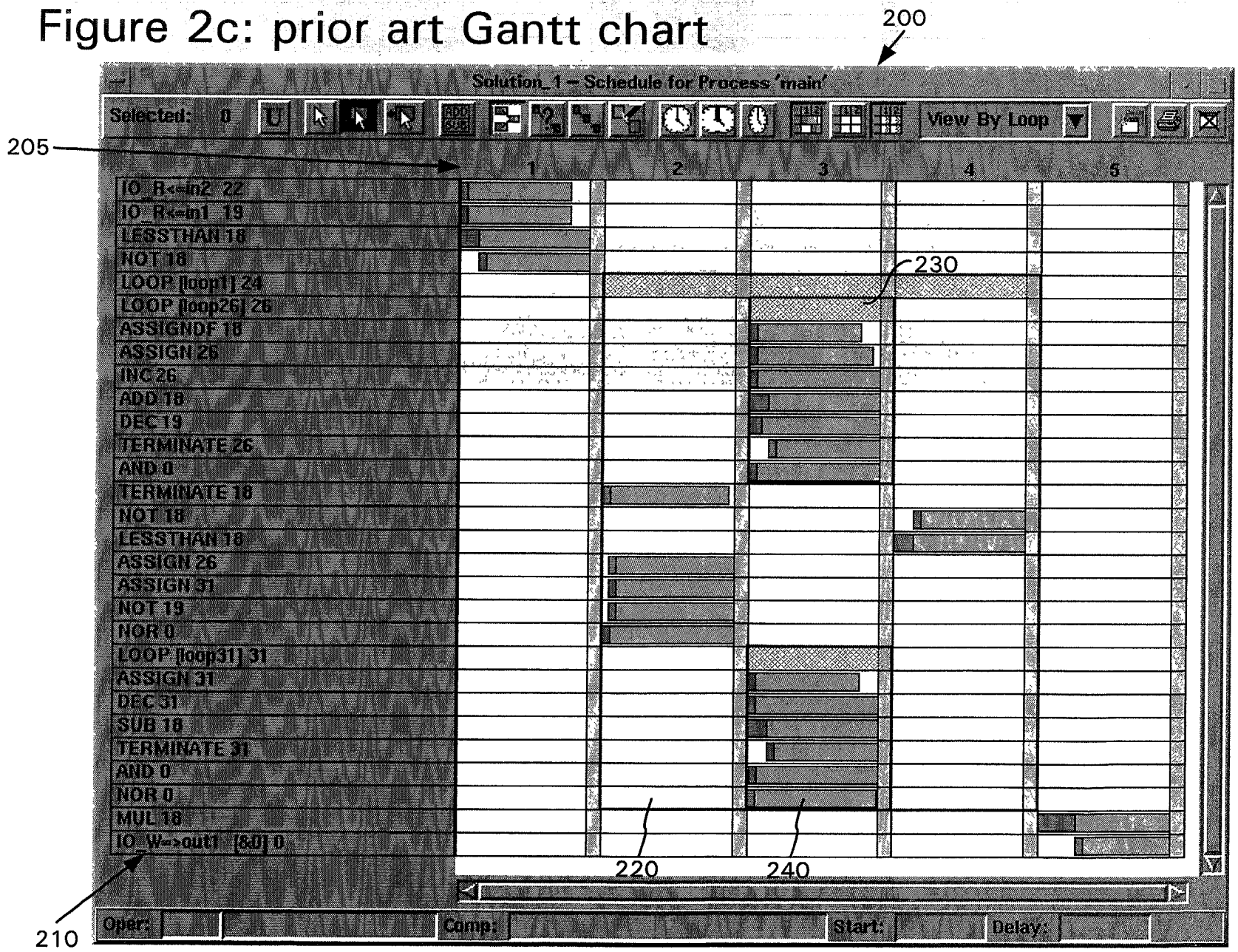
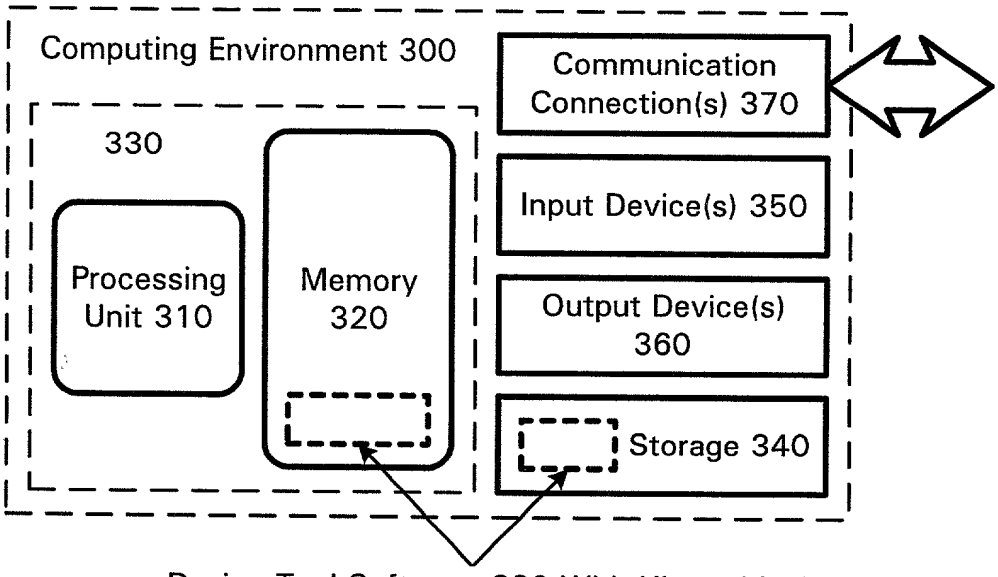


Figure 3



Design Tool Software 380 With Hierarchical Presentation of Scheduling Information

Figure 4

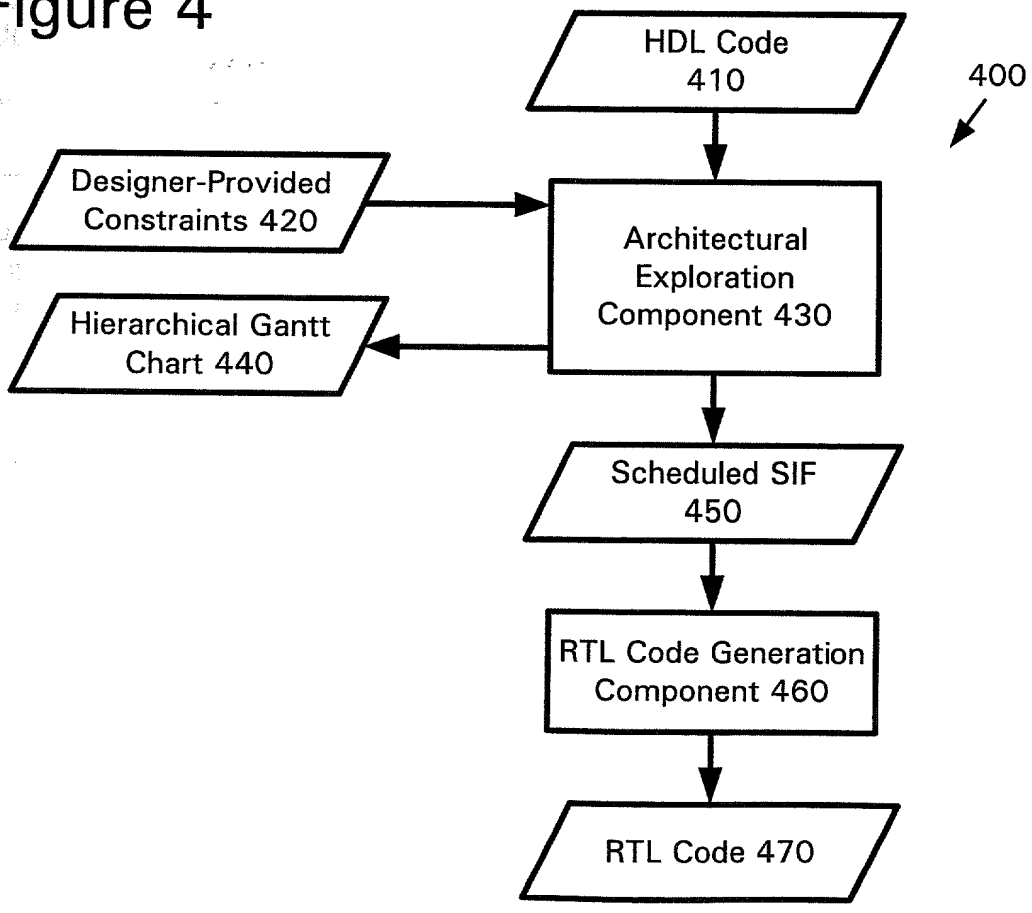


Figure 5

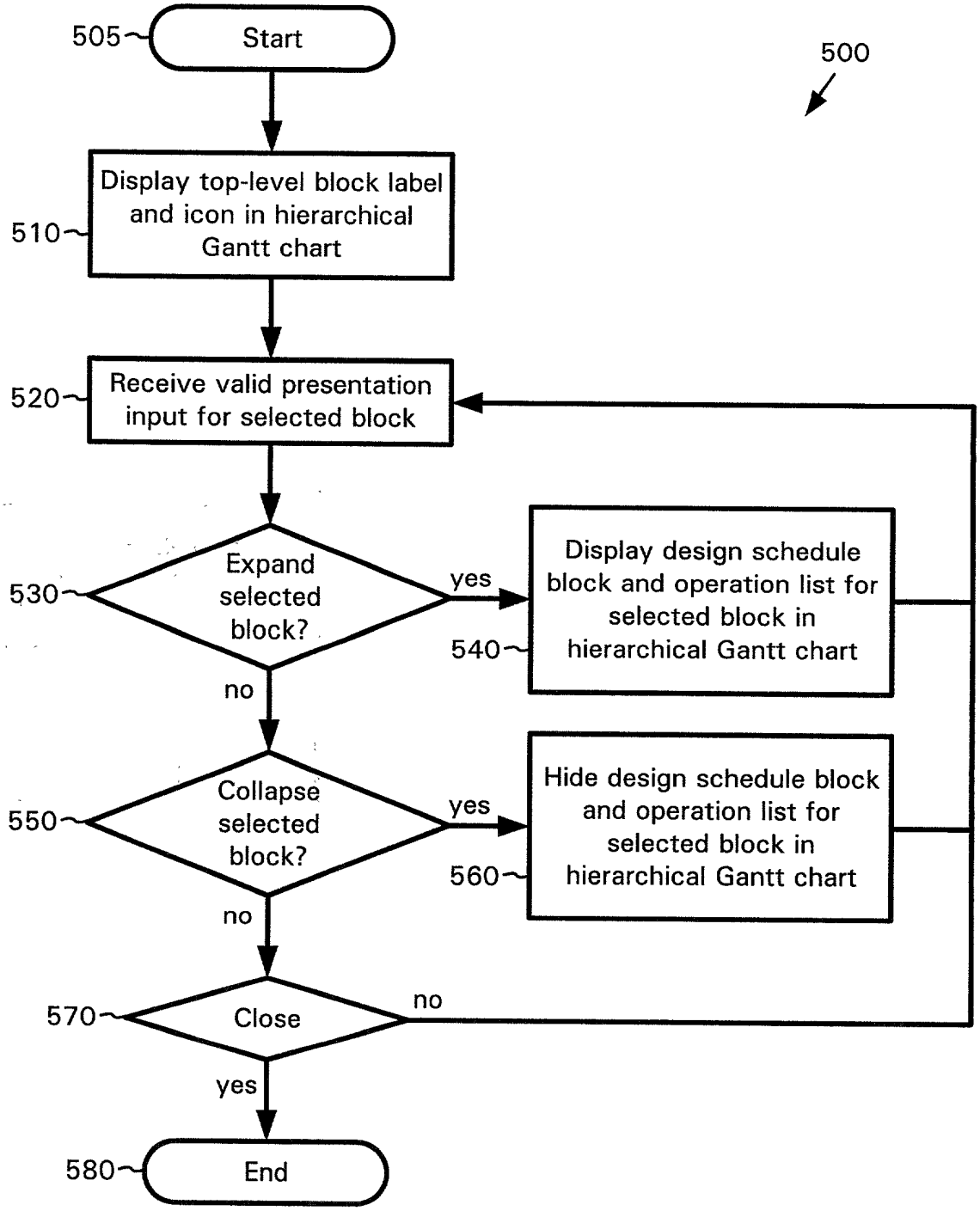

505
Start
500
Display top-level block label and icon in hierarchical Gantt chart
510
Receive valid presentation input for selected block
520
Expand selected block?
530
yes
Display design schedule block and operation list for selected block in hierarchical Gantt chart
540
no
Collapse selected block?
550
yes
Hide design schedule block and operation list for selected block in hierarchical Gantt chart
560
no
Close
570
no
yes
End
580

Figure 6a

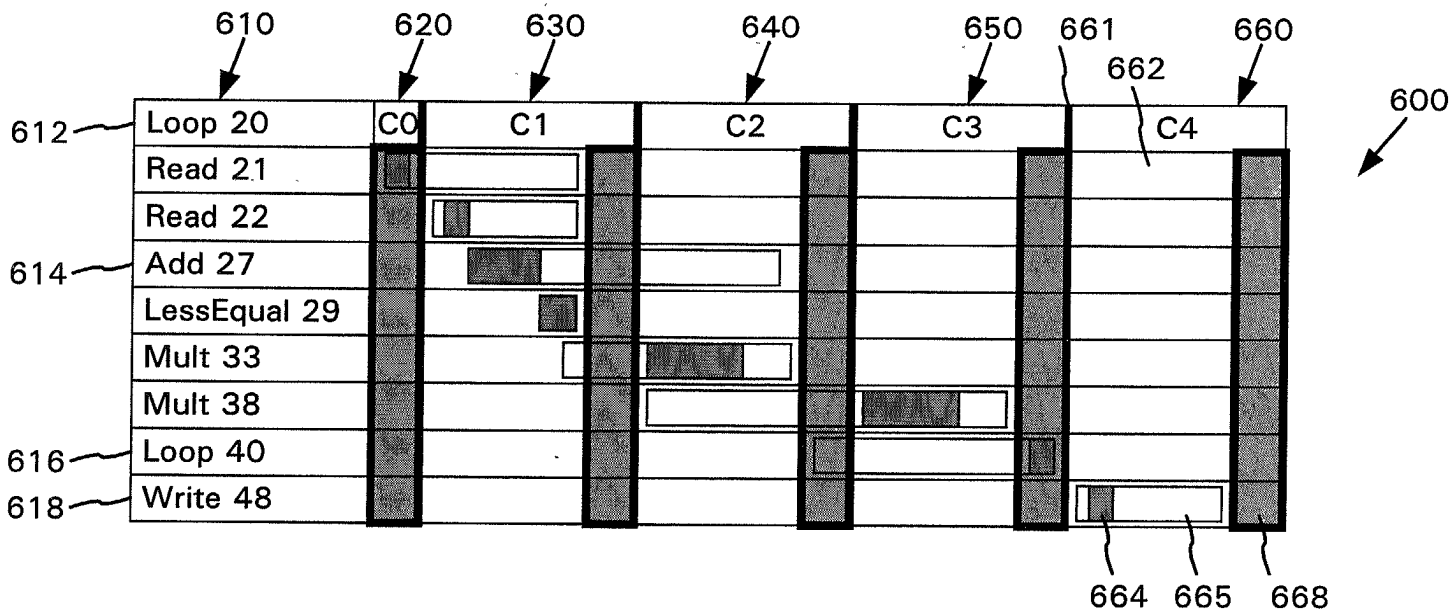


Figure 6b

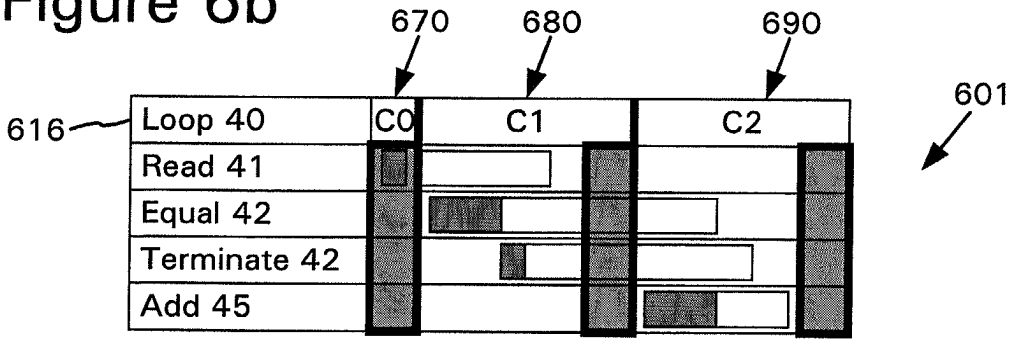


Figure 6c

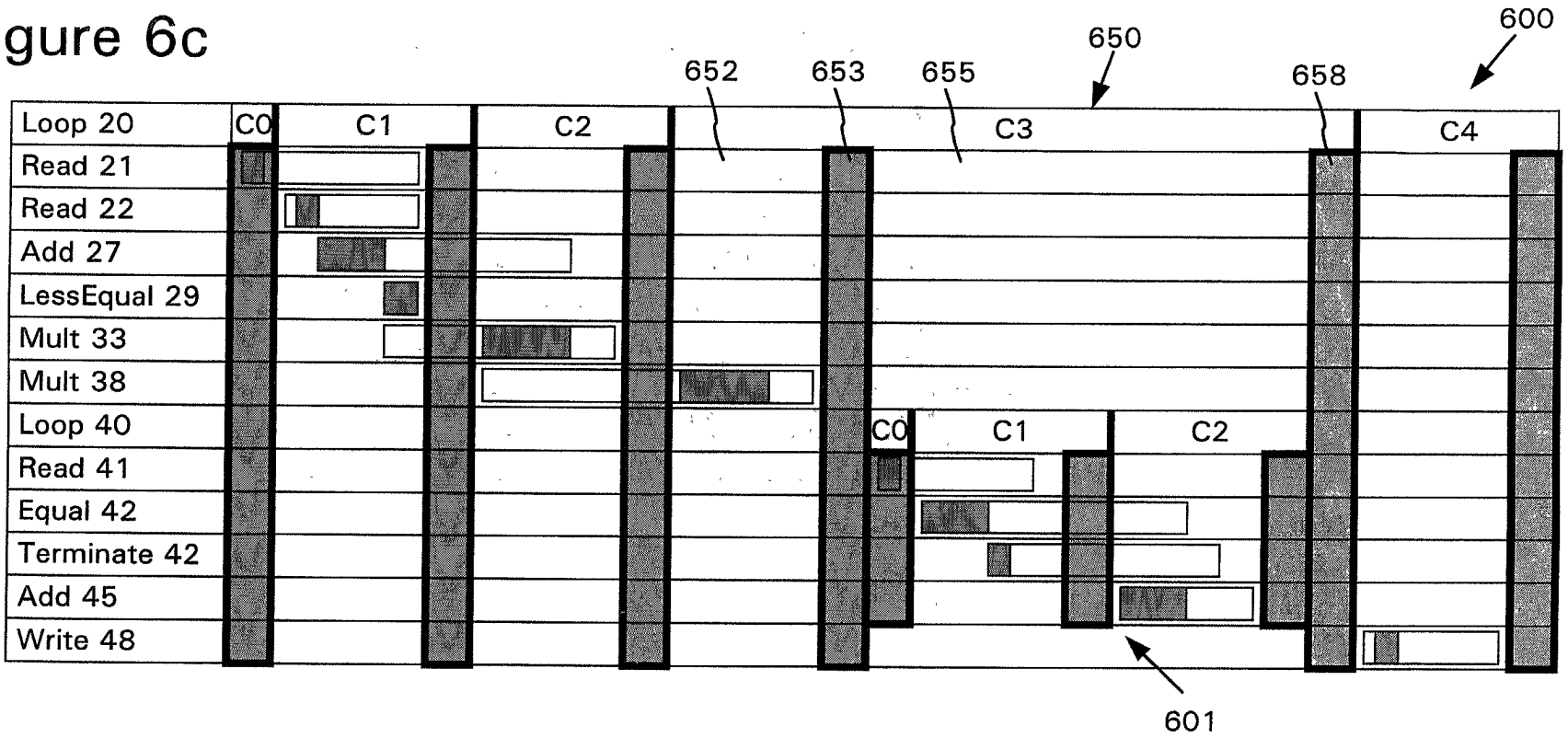


Figure 6d

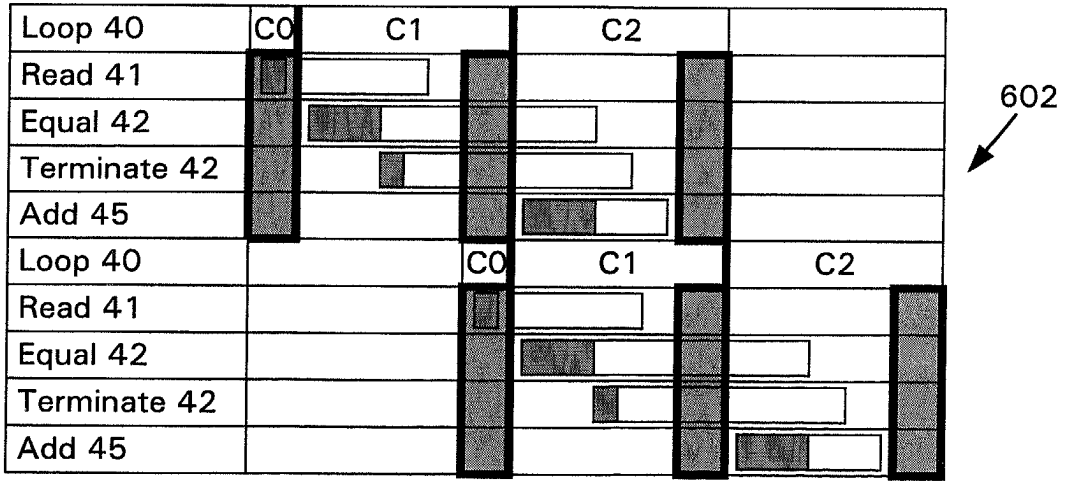


Figure 7a

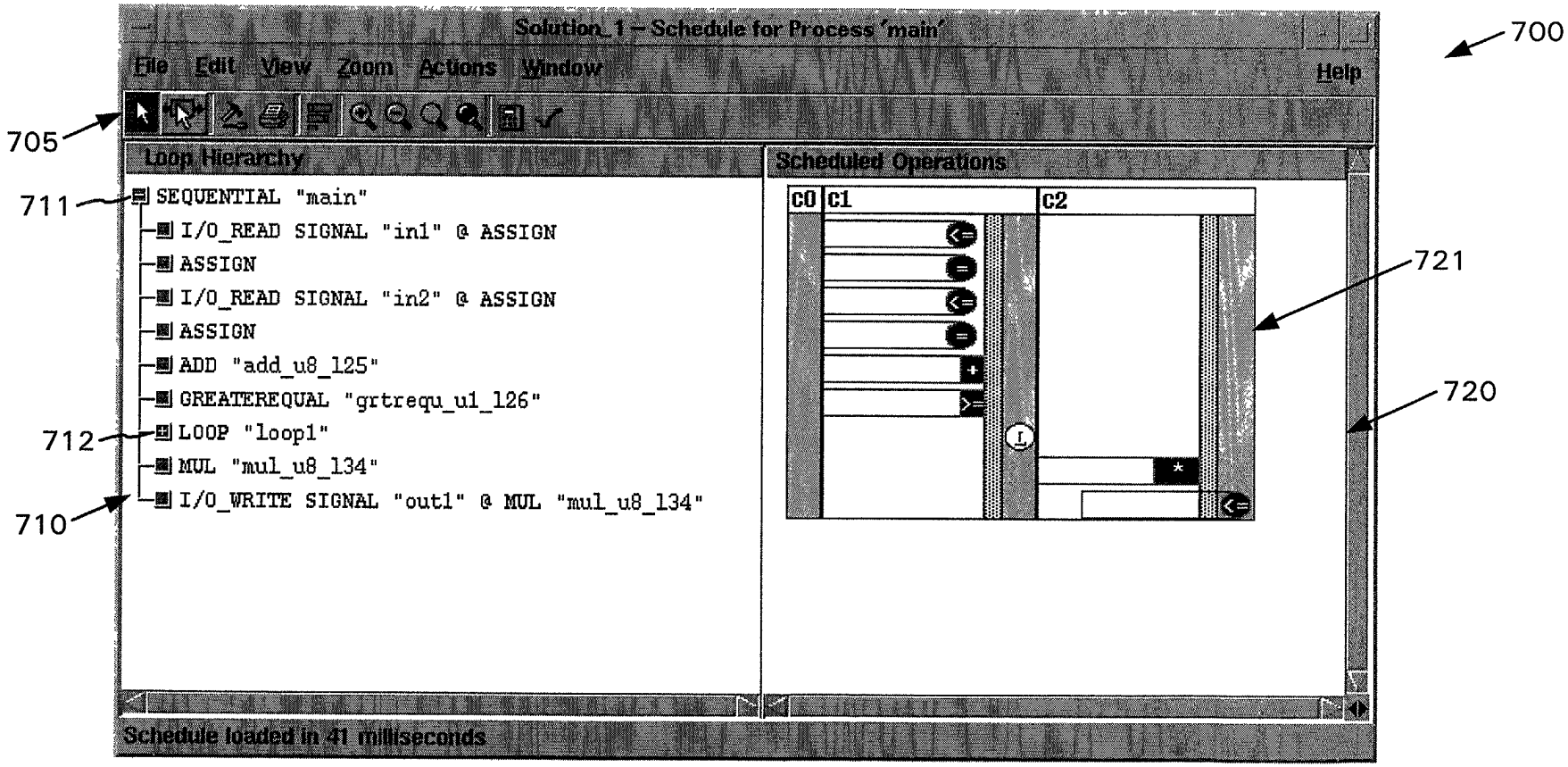

Solution_1 – Schedule for Process 'main'
File Edit View Zoom Actions Window Help
Loop Hierarchy
Scheduled Operations
SEQUENTIAL "main"
I/O_READ SIGNAL "in1" @ ASSIGN
ASSIGN
I/O_READ SIGNAL "in2" @ ASSIGN
ASSIGN
ADD "add_u8_125"
GREATEREQUAL "grtrequ_u1_126"
LOOP "loop1"
MUL "mul_u8_134"
I/O_WRITE SIGNAL "out1" @ MUL "mul_u8_134"
C0
C1
C2
Schedule loaded in 41 milliseconds
700
705
711
712
710
721
720

Figure 7b

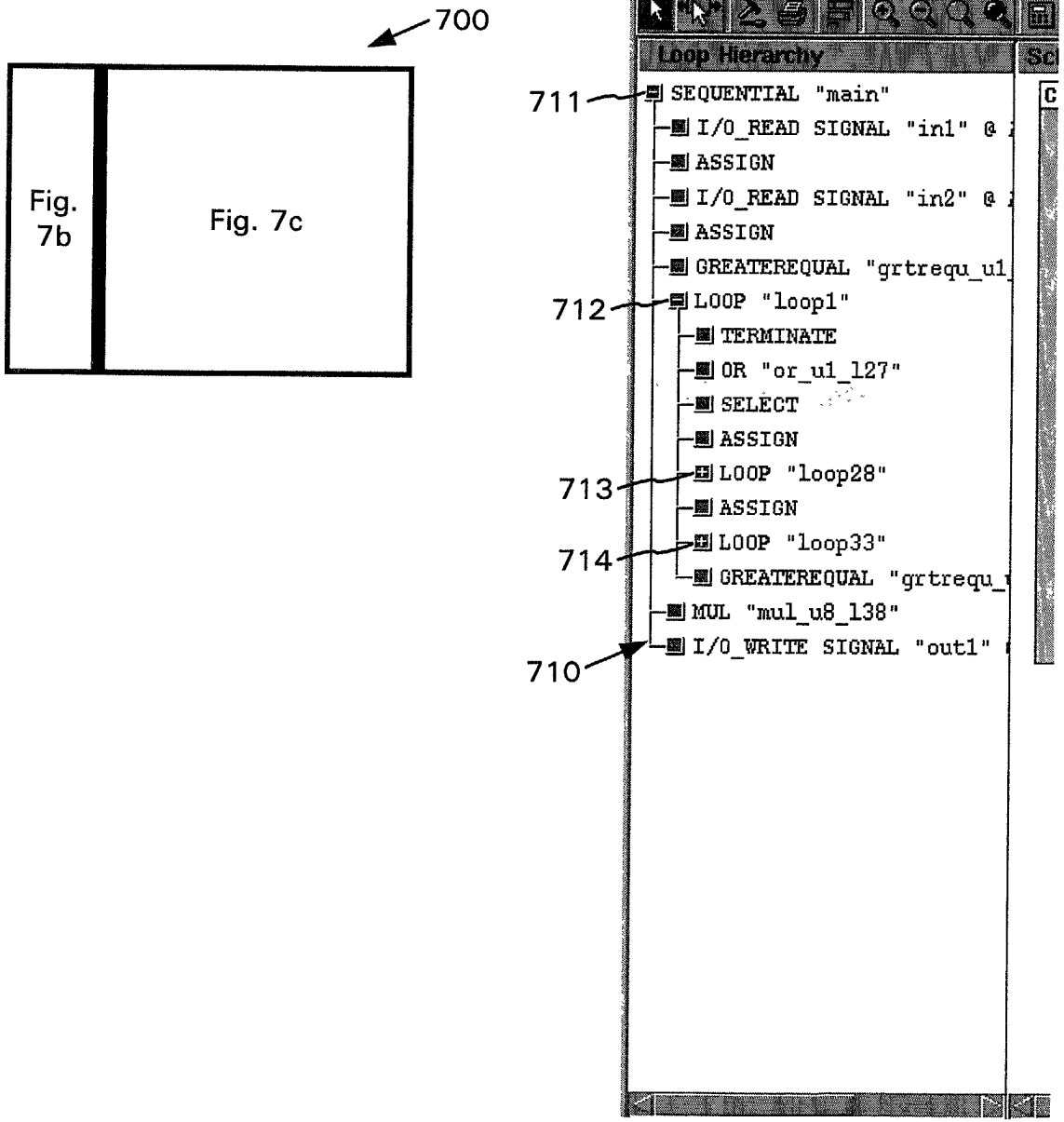

700
Fig. 7b
Fig. 7c
711
712
713
714
710
File Edit View Zoom Actions
Loop Hierarchy
SEQUENTIAL "main"
I/O_READ SIGNAL "in1" @
ASSIGN
I/O_READ SIGNAL "in2" @
ASSIGN
GREATEREQUAL "grtrequ_u1
LOOP "loop1"
TERMINATE
OR "or_u1_127"
SELECT
ASSIGN
LOOP "loop28"
ASSIGN
LOOP "loop33"
GREATEREQUAL "grtrequ_
MUL "mul_u8_138"
I/O_WRITE SIGNAL "out1"

Figure 7c

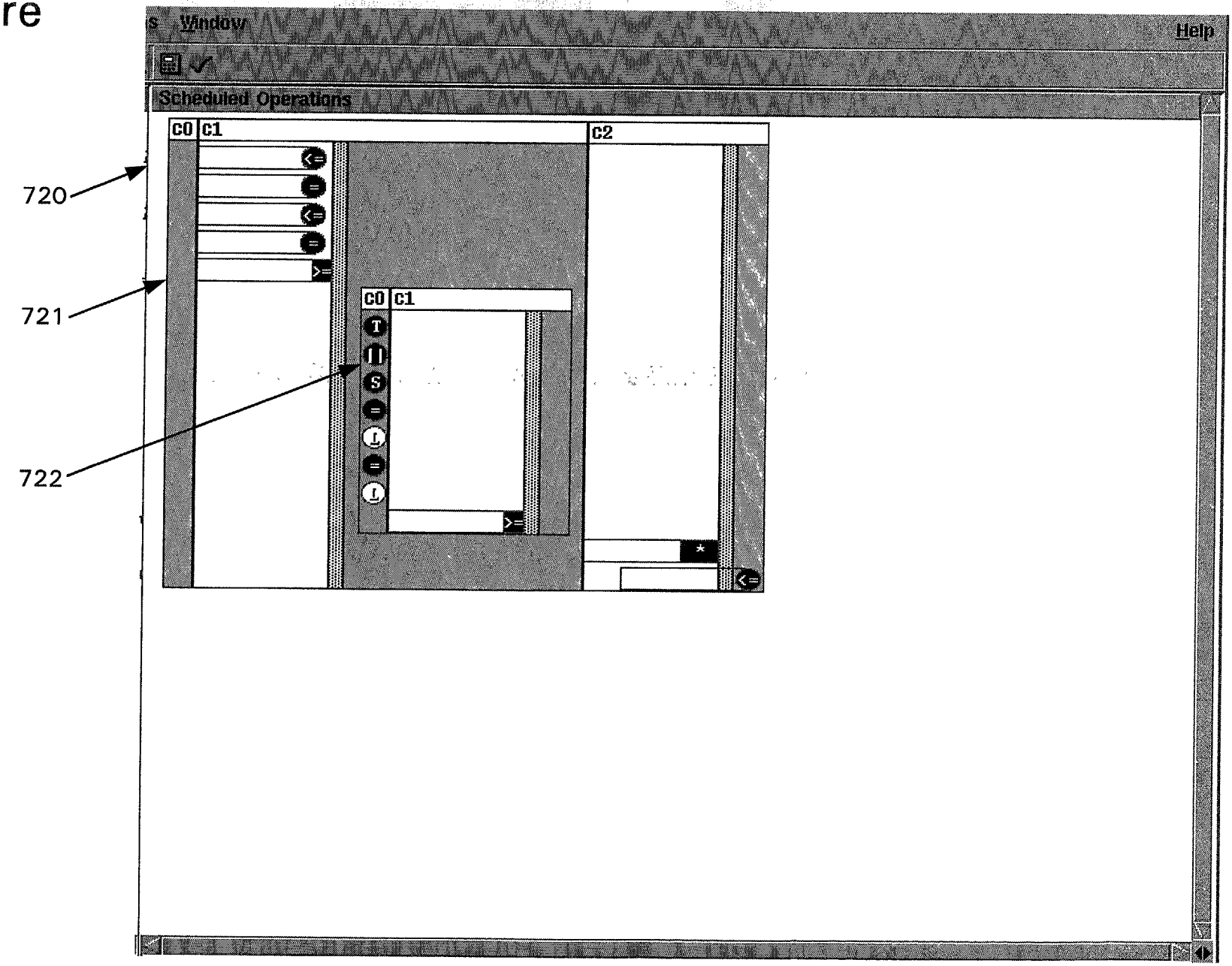
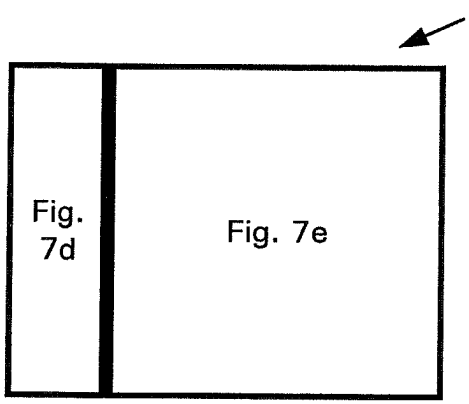


Figure 7d


700
Fig. 7d
Fig. 7e

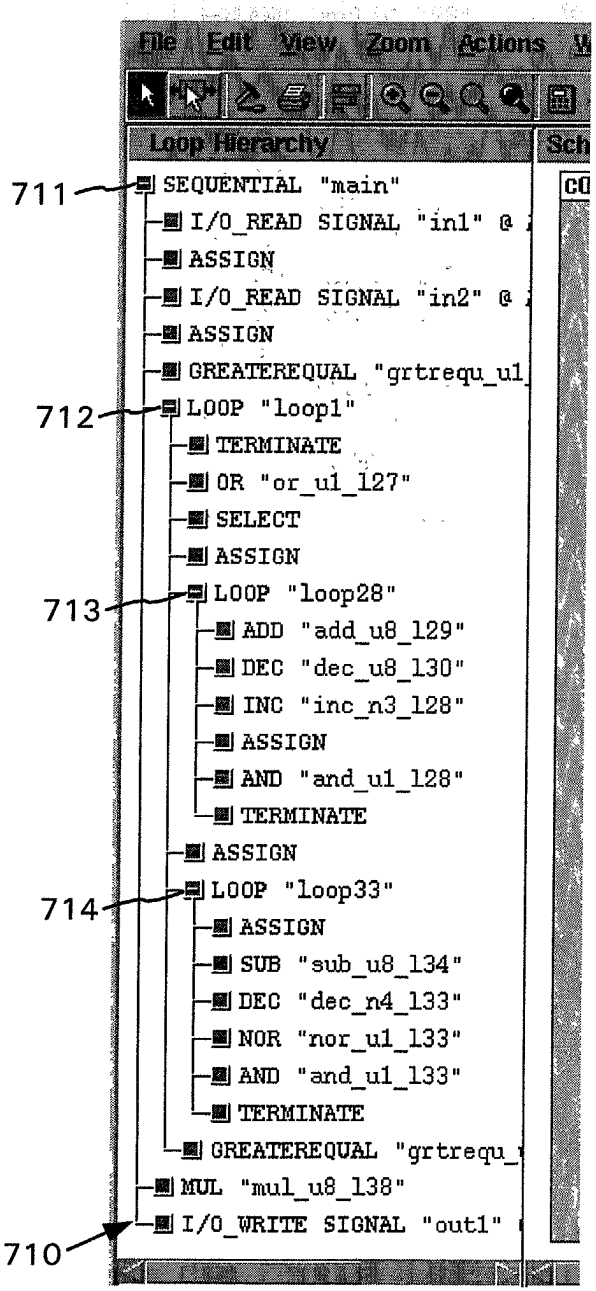
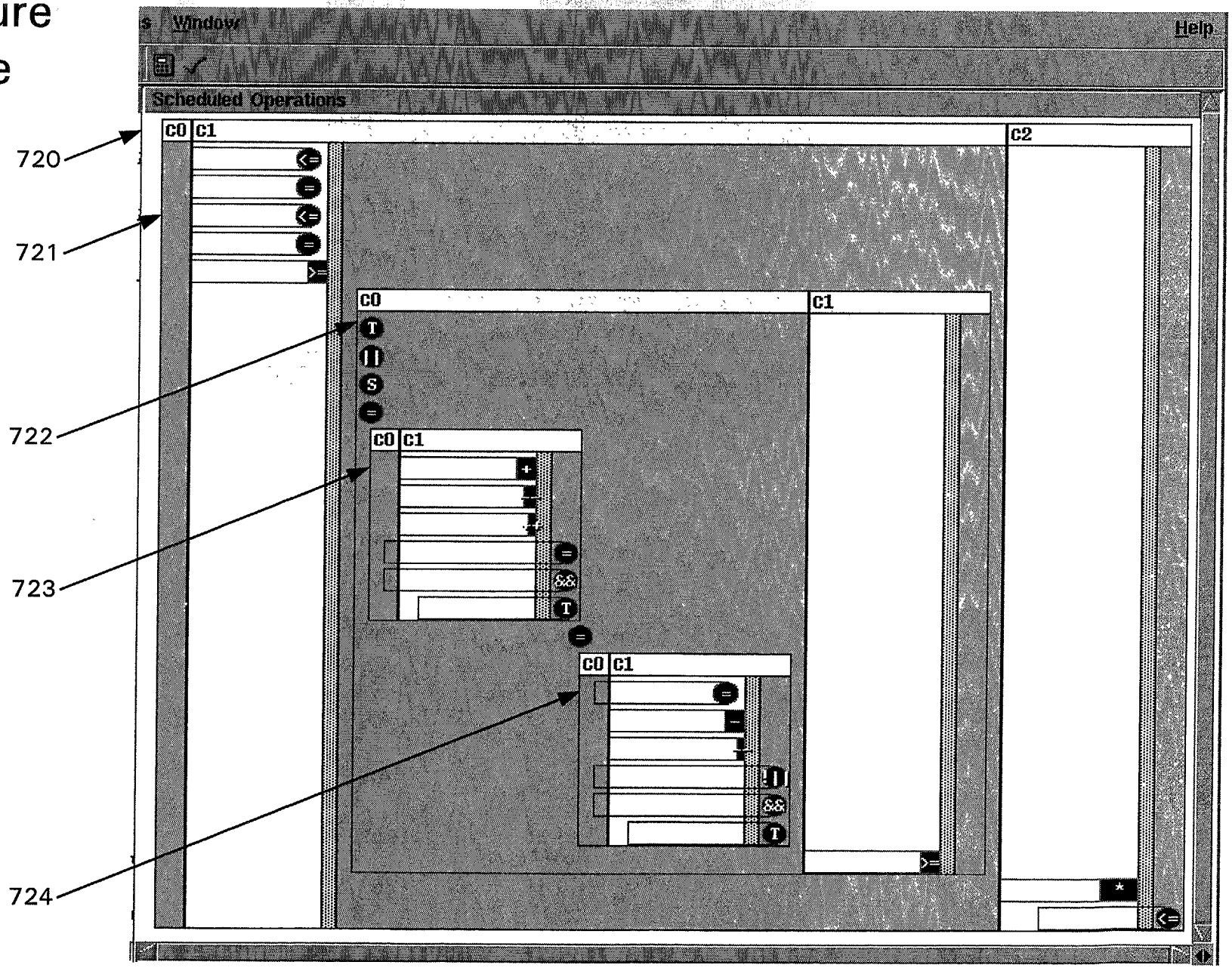

File Edit View Zoom Actions
Loop Hierarchy
711
SEQUENTIAL "main"
I/O_READ SIGNAL "in1" @
ASSIGN
I/O_READ SIGNAL "in2" @
ASSIGN
GREATEREQUAL "grtrequ_u1
712
LOOP "loop1"
TERMINATE
OR "or_u1_127"
SELECT
ASSIGN
713
LOOP "loop28"
ADD "add_u8_129"
DEC "dec_u8_130"
INC "inc_n3_128"
ASSIGN
AND "and_u1_128"
TERMINATE
ASSIGN
714
LOOP "loop33"
ASSIGN
SUB "sub_u8_134"
DEC "dec_n4_133"
NOR "nor_u1_133"
AND "and_u1_133"
TERMINATE
GREATEREQUAL "grtrequ_
MUL "mul_u8_138"
I/O_WRITE SIGNAL "out1"
710

Figure 7e


Window
Help
Scheduled Operations
C0
C1
C2
720
721
722
723
724